IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Wolfgang Hoess	Art Unit	: 2816
Patent No.	: 7,626,433	Examiner	: John W. Poos
Issue Date	: December 1, 2009	Conf. No.	: 1058
Serial No.	: 10/554,970		
Filed	: February 5, 2007		

Title : FLIP-FLOP CIRCUIT ASSEMBLY

Attn.: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF REQUEST FOR CERTIFICATE OF CORRECTION

Applicant hereby requests that a certificate of correction be issued for the above patent in accordance with the attached request.

All errors sought to be corrected were made in printing by the Patent and Trademark Office, and no fee is believed to be due.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: January 4, 2010

/Paul Pysher/

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transmittal of reque_1.doc

CERTIFICATE OF MAILING BY EFS-WEB FILING

I hereby certify that this paper was filed with the Patent and Trademark Office using the EFS-WEB system on this date: January 04, 2010

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. .: 7,626,433

APPLICATION NO .: 10/554,970

DATED .: DECEMBER 1, 2009

INVENTOR(S) .: WOLFGANG HOESS

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Cover page, Column 1, Line 1:
Delete [FLIP-FLOP CIRCUIT ASSEMBLY] and Insert - - FLIP-FLOP CIRCUIT THAT INCLUDES DIFFERENTIAL AMPLIFIERS- -

Cover page, Column 2, Abstract:
Delete [A flip-flop circuit arrangement having a total of four differential amplifiers (1, 2, 3, 4), which are connected to one another to produce a D flip-flop, is specified. According to the suggested principle, the two shared emitter nodes (E1, E2) of the differential amplifiers (1, 2, 3, 4) are connected via a switch pair (S1, S2) to supply potential and are activated by a differential input clock signal at a control input (CN, CP). The present flip-flop circuit is operable using especially low supply voltage (VCC) and is preferably suitable for constructing frequency dividers or shift registers.]
Insert - -A flip-flop circuit includes a first differential amplifier with first emitter-coupled transistors having emitters connected to a first emitter node, where the first emitter-coupled transistors include collector terminals that form at last parts of a first circuit node and a second circuit node, and base terminals that are cross-connected to collector terminals of the first emitter-coupled transistors. A second differential amplifier includes second emitter-coupled transistors having emitters connected to a second emitter node, where the second emitter-coupled transistors include collector terminals that are

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connected to the first circuit node and/or to the second circuit node, and base terminals that form at least part of a third circuit node and a fourth circuit node. A third differential amplifier includes third emitter-coupled transistors having emitters connected to the second emitter node, where the third emitter-coupled transistors include collector terminals that are connected to the third circuit node and/or to the fourth circuit node, and base terminals that are cross-connected to collector terminals of the third emitter-coupled transistors. A fourth differential amplifier includes fourth emitter-coupled transistors having emitters connected to the first emitter node, where the fourth emitter-coupled transistors include collector terminals that are connected to the third circuit node and/or to the fourth circuit node, and base terminals that are connected to the second circuit node and/or to the first circuit node; - -

Second page, Column 1, Line 1:
Delete [FLIP-FLOP CIRCUIT ASSEMBLY] and Insert - - FLIP-FLOP CIRCUIT THAT INCLUDES DIFFERENTIAL AMPLIFIERS- -

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